EE 330 Fall 2022
Homework 6 Solutions

Problem 1 : Assume a resistor has a resistance of 1kΩ at T = 300°k. If the TCR of this resistor is constant of value 2000ppm/°C, what will be the resistance at T = 350° k?

Solution

$$R(T_2) = R(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right] =$$

$$R(350°K) = R(300°K)\left[1 + (350-300)\frac{2000}{10^6}\right]$$

$$R(350°K) = 1000\left[1 + \left(50 \times \frac{2000}{10^6}\right)\right] = 1100\,\Omega = 1.1\,k\Omega$$

2.

We got the value of resistivity based on the doping density.

Doping density → $5 \times 10^{14}\ cm^{-3}$

Resistivity → 9.045 Ω-cm

$$R = \frac{\rho L}{WH} = \frac{9.045 \times 0.2}{0.015 \times 0.005} = 24.12k\,\Omega$$

Problem 3

From Lecture 13

$$R(T_2) = R(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right]$$

therefore,

$$R_1(T_2) + R_2(T_2) = R_1(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right] + R_2(T_1)\left[1 + (T_2 - T_1)\frac{TCR}{10^6}\right]$$

$$= R_1(T_1) + R_1(T_1)(T_2 - T_1)\frac{TCR}{10^6} + R_2(T_1) + R_2(T_1)(T_2 - T_1)\frac{TCR}{10^6}$$

$$= R_1(T_1) + R_2(T_1) + (T_2 - T_1)\left[R_1(T_1)\frac{TCR}{10^6} + R_2(T_1)\frac{TCR}{10^6}\right]$$

$$= 10 \times 10^3 + (T_2 - T_1)\left[3000\left(\frac{-1200}{10^6}\right) + 7000\left(\frac{800}{10^6}\right)\right]$$

$$= 10 \times 10^3 + 10 \times 10^3 (T_2 - T_1)\frac{200}{10^6} = 10 \times 10^3\left[1 + (T_2 - T_1)\frac{200}{10^6}\right]$$

This implies that the equivalent TCR is 200 ppm/°C

The TCR of the 10K resistor will be -1200ppm/C. We can say that the TCR of the series connection is lower than the TCR of the 10k resistor.

Problem 4 (a)

Using voltage divider, $V_{out} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_{in}$

3dB frequency = Cut off frequency = $f_c = 10MHz$

$\rightarrow f_c = \frac{1}{2\pi RC}$

$\rightarrow C = \frac{1}{2\pi R f_c} = \frac{1}{2\pi \times 10 \times 10^3 \times 10 \times 10^6} = 1.592 \times 10^{-12} = 1.592pF$

$\rightarrow$ Using $R(T_2) = R(T_1)\left[1 + (T_2 - T_1)\frac{2300}{10^6}\right]$

$C(T_2) = C(T_1)\left[1 + (T_2 - T_1)\frac{1000}{10^6}\right]$

the temperature value pairs for each resistor can be found as

$\rightarrow$ At 273K, $R = 10K\Omega$, $C = 1.592pF$ and the 3dB frequency = 10MHz

$\rightarrow$ At 350K, $R = 11.771K\Omega$, $C = 1.715pF$ and 3dB frequency = 7.88MHz

so the graphs will look as shown below with the 3dB frequency or cut off frequency as calculated above.

(b)

% change in 3dB frequency $= \frac{10MHz - 7.88MHz}{10MHz} \times 100\%$

$= 21.2\%$

5.

P5) What is the range in the diode current?

$I_D = J_s A \, e^{\frac{V_D}{nV_t}}$ $\quad V_D = 0.5V$ or 0.6

$J_s = 10^{-15} A/u^2$ $\quad V_t = 26mV$

$A = 50u^2$ $\quad n = 1$

0.5 V

$I_D = 10^{-15} \frac{A}{u^2} \cdot 50u^2 \; e^{\frac{0.5V}{26mV}}$

$I_D = 11.241 uA$

0.6V

$I_D = 10^{-15} A/u^2 \cdot 50u^2 \; e^{\frac{0.6V}{26mV}}$

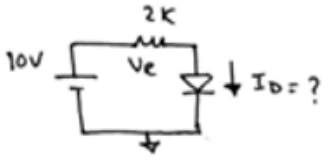
$I_D = 526.199 uA$

The range in the diode current is between

$11.241uA \sim 526.199uA$

P6.) Determine the current I_D. $V_x = 10V$ $\quad A = 200u^2$

$J_s = 10^{-15} A/u^2$ $\quad V_t = 26mV$



$V_x = I_D \cdot R + V_D$ $\quad V_D = 0.6V$

$\Rightarrow 10V = I_D \cdot 2K + 0.6V$

$I_D = \frac{10V - 0.6V}{2K} = 4.7mA$

Diode is "on"

$I_D = 4.7mA > 0$

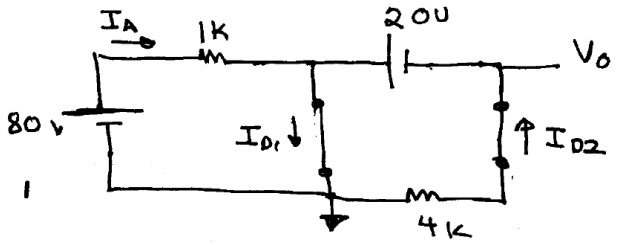
7). Since V_x is much smaller, it can be shown that the simplified diode models will not be good enough to accurately predict I_D so must use diode equation

$$520mV = I_D(2k) + V_D$$
$$I_D = J_s A\, e^{\frac{V_D}{nV_t}}$$

} eliminate V_D $\quad 520mV = 2kI_D + nV_t \ln\left(\frac{I_D}{J_s A}\right)$

with $n=1$, $V_t = 25mV$ and $J_s A = 2E-14$, solving iteratively for I_D we obtain $I_D = 26.5\mu A$

8) For circuit on left Guess D1 and D2 ON.



To verify guess, must show $I_{D1} > 0$ & $I_{D2} > 0$

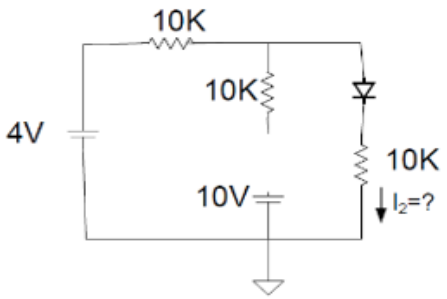
solving, obtain $V_o = -20V$. must now verify

$$I_{D2} = \frac{20V}{4k} = 5mA \qquad I_{D1} = I_A + I_{D2} = \frac{80V}{1k} + 5mA = 85mA$$

thus $I_{D1} > 0$ & $I_{D2} > 0$ so $V_o = -20V$ solution is valid

For the right circuit:

I will start by assuming the middle diode is off, and the rightmost diode is on. This guess is made on the assumption that the location of the 10V source relative to the 4V source will cause currents to flow in the wrong directions. This allows us to treat the middle diode as an open circuit, giving us the following diagram.



As the 10V source drives an open circuit and the 10kΩ resistor ends at an open circuit, we can neglect them. Using KVL, we can find the current through the loop using the following equation:

$$4V - (i_2 * 10k\Omega) - 0.7V - (i_2 * 10k\Omega) = 0$$

This should reduce down to $i_2 = \frac{3.3V}{20k\Omega} = 165\mu A$, which gives a 1.65V drop across each resistor. Additionally, this gives a voltage of 2.35V at the anode of the rightmost diode. With the 10V source at the cathode of the middle diode, this would make the voltage across the middle 10kΩ resistor and diode -7.65V, meaning current would be flowing the wrong direction through the diode and confirming the initial assumption that it is off. This gives us the result of $i_2 = 165\mu A$.

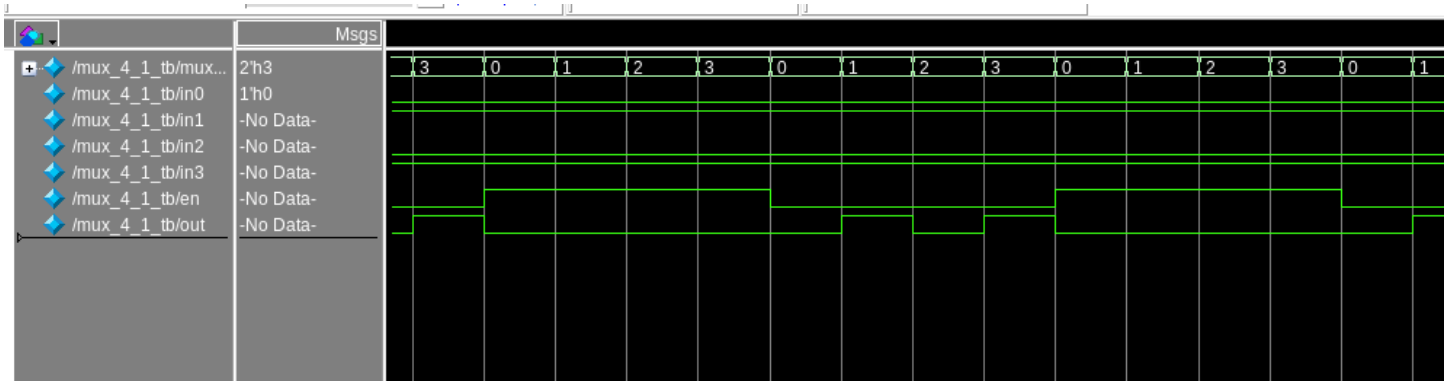
9/10.

/home/ha1207/ee465_verilog/mux.v - Default

Ln#

```
1  `timescale 1ns/1ps
2  module mux4_1(in0,in1,in2,in3,en,mux_sel,out);          //initiation of module
3
4          input in0,in1,in2,in3,en;                       //initiation of input bits
5          input [1:0] mux_sel;                            //initiation of select pin for mux
6          output reg out;                                 // initiation of output
7
8          always @(*)begin                                //starts for any change values
9          if (en)          begin                          //active low input =1
10                          out = 0;                       //active low output
11                         end
12         else
13                         begin
14                         case(mux_sel)                   // for selecting a mux pin
15
16                         2'b00 : out = in0;              //assigning values based on select pin
17                         2'b01 : out = in1;
18                         2'b10 : out = in2;
19                         2'b11 : out = in3;
20                         endcase
21
22                         end
23
24         end
25
26 endmodule
27
```

```
Ln#
 1  `timescale 1ns/1ps
 2  module mux_4_1_tb();
 3
 4          reg [1:0] mux_sel;                      //inputs are initiated as registers
 5
 6          reg in0,in1,in2,in3,en;
 7
 8          wire out;                               //outputs are initiated  as wires
 9
10          mux4_1 dut(in0,in1,in2,in3,en,mux_sel,out);     //initiation of dut
11
12                  initial in0 = 0;
13                  initial in1 = 1;
14                  initial in2 = 0;
15                  initial in3 = 1;
16                  initial en = 0;
17                  initial mux_sel = 2'b00;
18
19                  always #1 mux_sel[0] = ~mux_sel[0];
20                  always #2 mux_sel[1] = ~mux_sel[1];
21
22                  always #4 en = ~en;
23
24  endmodule
25
26
```

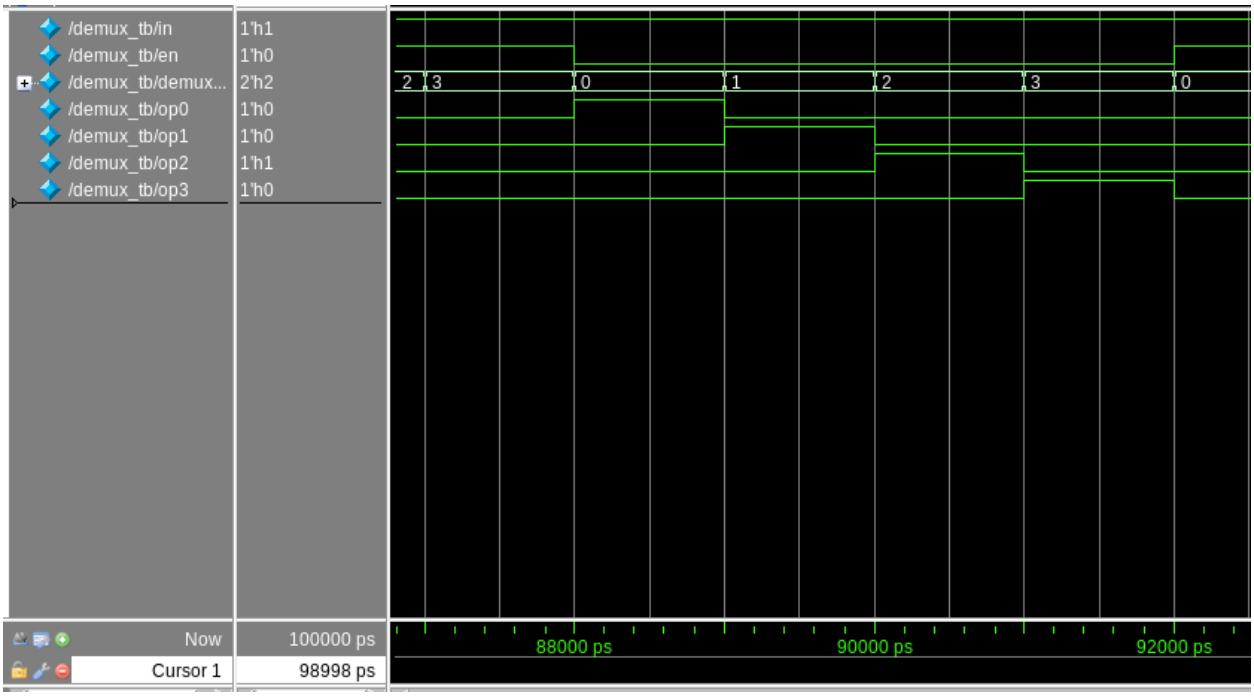


```
module demux4_1(in,op0,op1,op2,op3,demux_sel,en);        //initiation of module

        input in,en;                                     //initiation of input pins
        input [1:0] demux_sel;                           //intitiation of select pin for demux output

        output reg op0,op1,op2,op3;                      //initiation of outputs

        always @(*) begin                                // starts for any change in values
                        if (en) begin                    // active low input = 1
                                op0 = 0;
                                op1 = 0;
                                op2 = 0;
                                op3 = 0;
                                end

                        else    begin
                                case(demux_sel)          //for different selections the output is
                                2'b00:begin              // received at a different pin
                                op0 = in;
                                op1 = 0;
                                op2 = 0;
                                op3 = 0;
                                        end
                                2'b01:begin
                                op0 = 0;
                                op1 = in;
                                op2 = 0;
                                op3 = 0;
                                        end
                                2'b10:begin
                                op0 = 0;
                                op1 = 0;
                                op2 = in;
                                op3 = 0;
                                        end
                                2'b11:begin
                                op0 = 0;
                                op1 = 0;
                                op2 = 0;
                                op3 = in;
                                        end


                                endcase
                                end
                end
endmodule
```

/home/ha1207/ee465_verilog/demux_tb.v (/demux_tb) - Default *:

Ln#

```
1   `timescale 1ns/1ps
2
3   module demux_tb();
4
5   reg in, en;                                          //inputs are initiated as registers
6   reg [1:0] demux_sel;
7
8   wire op0,op1,op2,op3;                                //outputs are initiated as wires
9
10          demux4_1 dut(in,op0,op1,op2,op3,demux_sel,en);  //initiation of dut
11                  initial in =1;
12                  initial en =0;
13
14                  initial demux_sel = 2'b00;
15
16                  always #1 demux_sel[0] = ~demux_sel[0]; //toggle the bit 0 every cycle
17                  always #2 demux_sel[1] = ~demux_sel[1]; //toggle the bit 1 every 2 cycles
18
19                  always #4 en = ~en;                  //toggle the enable pin every 4 clock cycles
20
21  endmodule
22
```


/demux_tb/in
/demux_tb/en
/demux_tb/demux...
/demux_tb/op0
/demux_tb/op1
/demux_tb/op2
/demux_tb/op3
1'h1
1'h0
2'h2
1'h0
1'h0
1'h1
1'h0
2
3
0
1
2
3
0
Now
100000 ps
Cursor 1
98998 ps
88000 ps
90000 ps
92000 ps